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EXAMINER	
LEE, EUGENE	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/475,452	MURTHY ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/13/04*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-6 and 8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, and 8 thru 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schunke et al. 5,814,861. Schunke discloses (see, for example, FIG. 4) a transistor (device) comprising a gate dielectric, substrate (first conductivity region of a substrate), gate electrode, pair of sidewall spacers, and source and drain regions (a pair of silicon or silicon alloy inwardly concaved source/drain region of a second conductivity type formed in said substrate). The source and drain regions are inwardly concaved and bend (inflection points) directly underneath the gate electrode. The channel region 5 directly beneath the gate electrode is larger that the channel region between the inflection points.

Schunke does not disclose an inflection point which occurs between 50-250 A laterally beneath said gate electrode and at a depth of between 25-100 A beneath said gate dielectric. However, the depth of the source/drain junctions and the distance between the inflection point and the gate electrode and gate dielectric are result effective variables that one of ordinary skill in the art would optimize for affecting the channel region in a field effect transistor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have an inflection point which occurs between 50-250 A laterally beneath said gate electrode and at a depth of between 25-100 A beneath said gate dielectric, in order to form a channel region,

and since it has been held that discovering the optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 F. 2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claims 8 and 9, Schunke discloses the claimed invention except for the first conductivity type being n-type conductivity and wherein said second conductivity type being p-type conductivity and vice versa. However, a transistor is a semiconductor device wherein the source and drain regions of one type are formed opposite to the type in a substrate. The opposite types are necessary in order to form a pn junction in the transistor so that a channel can be formed. Whether the source and drain regions are p or n type depends on whether a p-channel or n-channel transistor is formed. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have the first conductivity type being n-type conductivity and wherein said second conductivity type being p-type conductivity and vice versa in order to form a p or n-channel transistor, and since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claims 10 and 11, Schunke does not disclose the concentration of said deposited silicon or silicon alloy source/drain regions of a second conductivity type having a concentration between $1X10^{18}$ / cm^3 – $3X10^{21}$/ cm^3 or approximately $1X10^{21}$ / cm^3. However, it would have been obvious to one of ordinary skill in the art at the time of invention was made to use these concentrations in order to form source and drain regions that are capable of forming a channel therebetween, and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schunke et al. '861 as applied to claims 1, and 8-11 above, and further in view of Takeuchi 5,970,351. Schunke does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric. However, Takeuchi discloses (see, for example, FIG. 11 (c)) a MOSFET comprising elevated source and drain regions 7B with a facet structure. In column 12, lines 45-63, Takeuchi teaches that such a structure provides reduced parasitic capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric in order to reduce parasitic capacitance.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schunke et al. '861 as applied to claims 1, and 8-11 above, and further in view of Choi 6,057,582. Schunke does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a gate dielectric layer

being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode in order to reduce hot carrier effects.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schunke et al. '861 in view of Takeuchi '351 as applied to claim 2 above, and further in view of Choi 6,057,582. Schunke in view of Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a gate dielectric layer being thicker beneath the outside edge of said gate electrode than the gate dielectric layer beneath the center of said gate electrode in order to reduce hot carrier effects.

6. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schunke et al. '861 as applied to claims 1, and 8-11 above, and further in view of Choi et al. 5,793,088. Schunke does not disclose a pair of deposited silicon or silicon alloy regions having a first conductivity type formed between said pair of deposited silicon or silicon alloy source/drain regions of said second conductivity type and said first conductivity type region. However, Choi discloses (see, for example, FIG. 2 and FIG. 3) a structure 106 comprising halo regions 120, 122. Choi teaches that halo regions provide higher punchthrough voltage. Therefore, it would have

been obvious to one of ordinary skill in the art at the time of invention to use halo regions in order to attain a higher punchthrough voltage.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schunke et al. '861 as applied to claims 1, and 8-11 above, and further in view of Hwang 5,567,966. Schunke does not disclose a silicide formed on said silicon or silicon alloy source/drain regions. However, Hwang discloses (see, for example, Fig. 6) a transistor comprising source and drain regions 24, and $TiSi_2$ regions (silicide) 20. In column 2, lines 17-19, Hwang teaches reduced source/drain resistance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a silicide formed on said silicon or silicon alloy source/drain regions in order to reduce resistance.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schunke et al. 5,814,861 in view of Wieczorek et al. 6,274,894 B1 in view of Takeuchi 5,970,351. Schunke discloses (see, for example, FIG. 4) a transistor (device) comprising a gate dielectric, substrate (first conductivity region of a substrate), gate electrode, pair of sidewall spacers, and source and drain regions (a pair of silicon or silicon alloy inwardly concaved source/drain region of a second conductivity type formed in said substrate). The source and drain regions are inwardly concaved and bend (inflection points) directly underneath the gate electrode. The channel region 5 directly beneath the gate electrode is larger that the channel region between the inflection points. Schunke does not disclose silicon-germanium alloy source/drain regions. However, Wieczorek discloses (see, for example, column 6, lines 8-23) that SiGe (silicon-germanium) in the

source/drain regions have a lower bandgap, which lowers contact resistance. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to use silicon-germanium alloy in order to lower contact resistance.

Schunke in view of Wieczorek does not disclose the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric. However, Takeuchi discloses (see, for example, FIG. 11 (c)) a MOSFET comprising elevated source and drain regions 7B with a facet structure. In column 12, lines 45-63, Takeuchi teaches that such a structure provides reduced parasitic capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have the source/drain regions extending above the gate dielectric and wherein the top surface of said silicon or silicon alloy is spaced further from said gate electrode than the silicon or silicon alloy adjacent to said gate dielectric in order to reduce parasitic capacitance.

9. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schunke et al. '861 in view of Wieczorek et al. '894 B1 in view of Takeuchi '351 as applied to claim 13 above, and further in view of Choi 6,057,582. Schunke in view of Wieczorek in view of Takeuchi does not disclose a gate dielectric layer being thicker beneath the outside edges of said gate electrode than the gate dielectric layer beneath the center of said gate electrode. However, Choi discloses (see, for example, FIG. 2) a semiconductor device comprising a gate insulating film with both sides thicker than a thickness in the center. Choi teaches (see, for example, abstract) that such a gate insulating film reduces hot carrier effects. Therefore it would have been obvious to one of

ordinary skill in the art at the time of invention to have a gate dielectric layer being thicker beneath the outside edges of said gate electrode than the gate dielectric layer beneath the center of said gate electrode in order to reduce hot carrier effects.

OPTIMIZATION OF RANGES

A. Optimization Within Prior Art Conditions or Through Routine Experimentation

Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955) (Claimed process which was performed at a temperature between 40°C and 80°C and an acid concentration between 25% and 70% was held to be prima facie obvious over a reference process which differed from the claims only in that the reference process was performed at a temperature of 100°C and an acid concentration of 10%.); >see also Peterson, 315 F.3d at 1330, 65 USPQ2d at 1382 ("The normal desire of scientists or artisans to improve upon what is already generally known provides the motivation to determine where in a disclosed set of percentage ranges is the optimum combination of percentages.");< ** In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969) (Claimed elastomeric polyurethanes which fell within the broad scope of the references were held to be unpatentable thereover because, among other reasons, there was no evidence of the criticality of the claimed ranges of molecular weight or molar

proportions.). For more recent cases applying this principle, see Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989); In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and In re Geisler, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

B. Only Result-Effective Variables Can Be Optimized

A particular parameter must first be recognized as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977) (The claimed wastewater treatment device had a tank volume to contractor area of 0.12 gal./sq. ft. The prior art did not recognize that treatment capacity is a function of the tank volume to contractor ratio, and therefore the parameter optimized was not recognized in the art to be a result-effective variable.). See also In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980) (prior art suggested proportional balancing to achieve desired results in the formation of an alloy).

Response to Arguments

10. Applicant's arguments with respect to claims 1-6, and 8-14 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the applicant's argument on page 7 that the cited references fail to teach an inflection point, which occurs between 50-250 A laterally beneath the gate electrode and at a depth of between 25-200 A beneath the gate dielectric, this argument is not persuasive. Schunke

clearly discloses (see, for example, FIG. 2)) a bending (inflection point) beneath the gate electrode 1 and gate dielectric 2. Even though Schunke does not disclose the specific distances associated with inflection point, the distances are result effect variables that one of ordinary skill in the art at the time of invention would optimize in order to form a channel region in a transistor.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
November 19, 2004

Tom Thomas

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